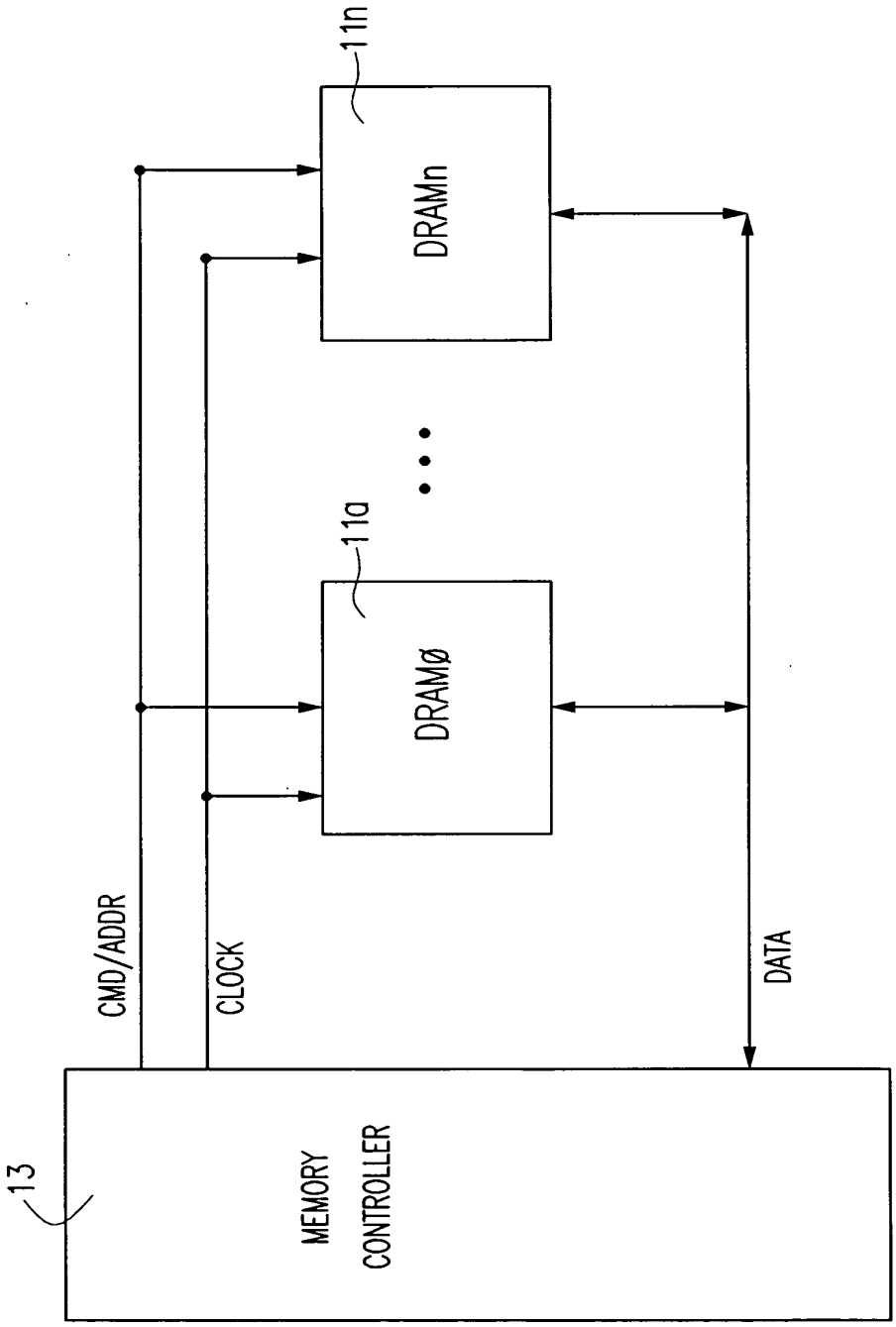
11n
DRAMn
11a
DRAMø
CMD/ADDR
CLOCK
DATA
13
MEMORY CONTROLLER

FIG. 1

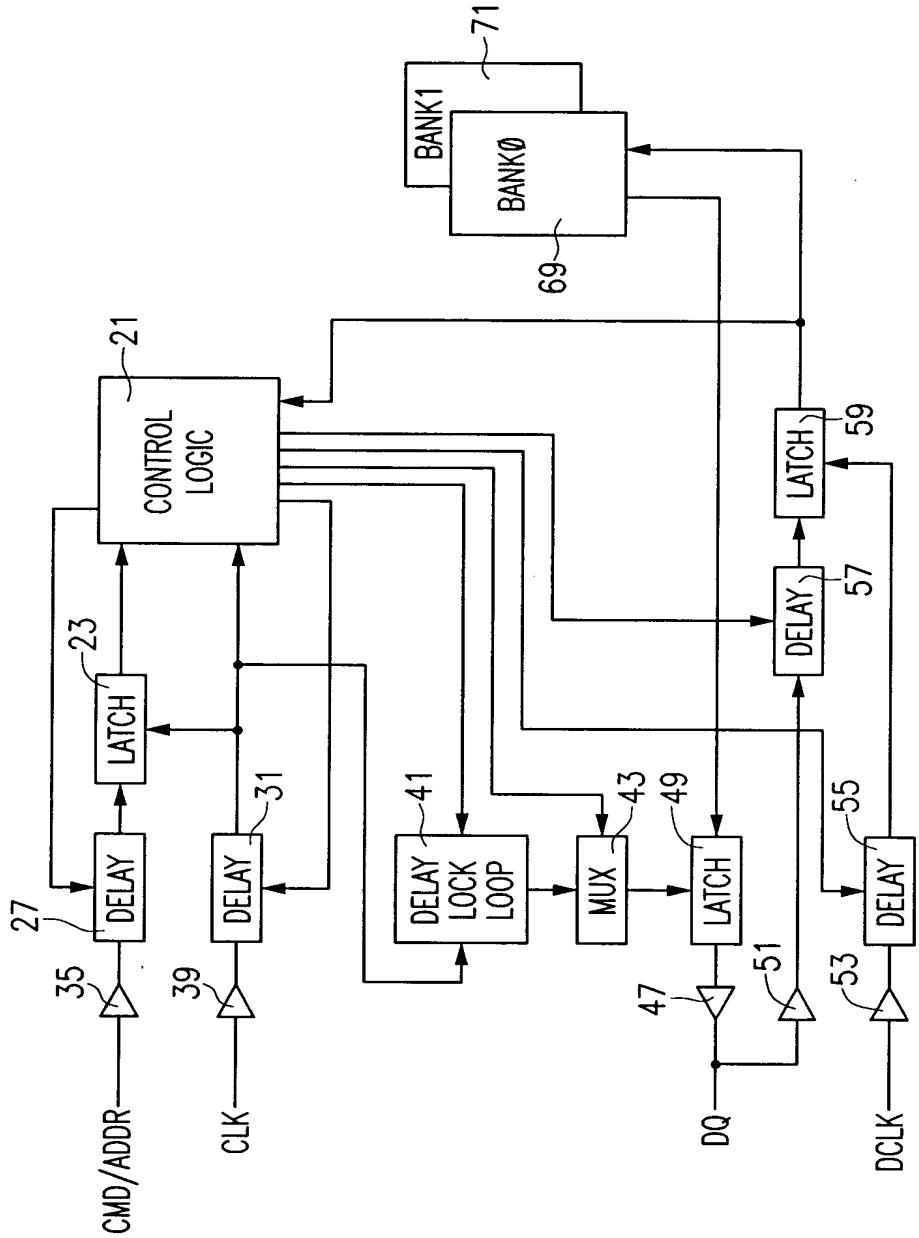
71
BANK1
BANK0
69
21
CONTROL LOGIC
59
LATCH
57
DELAY
23
LATCH
31
41
43
49
55
27
DELAY
DELAY
DELAY LOCK LOOP
MUX
LATCH
DELAY
35
39
47
51
53
CMD/ADDR
CLK
DQ
DCLK

FIG. 2

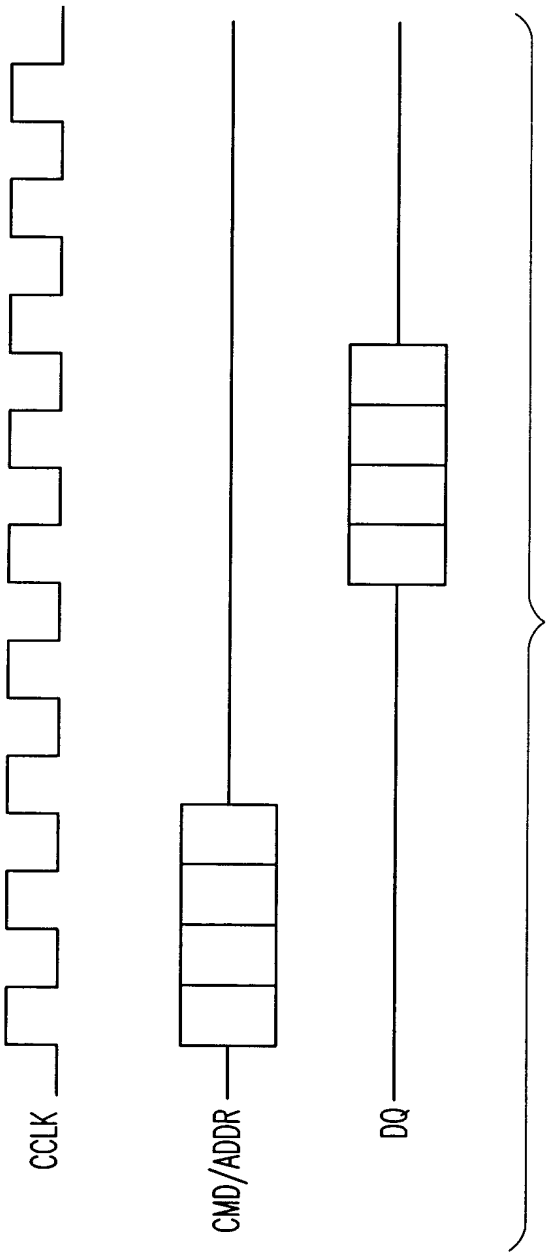

FIG. 3

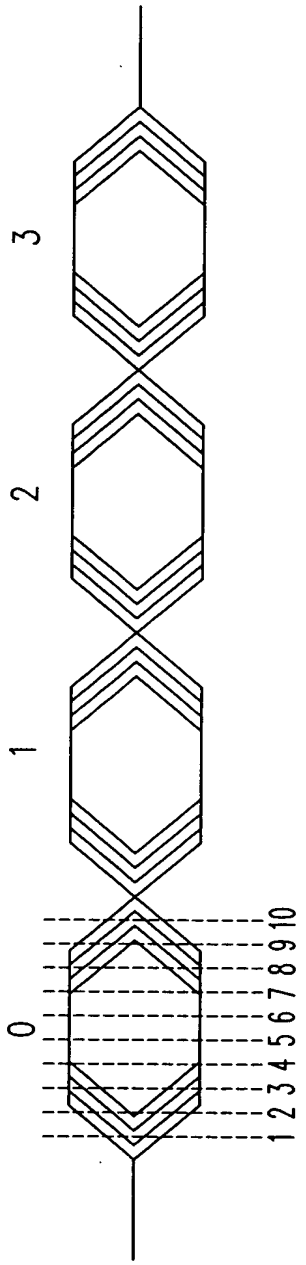

FIG. 4

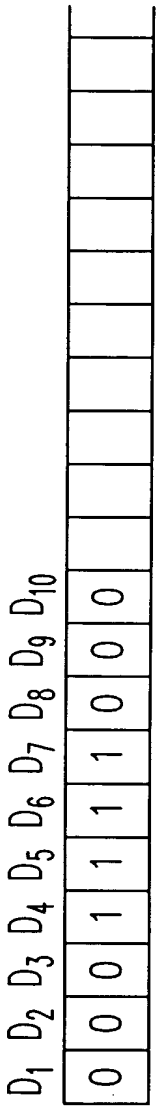

FIG. 5

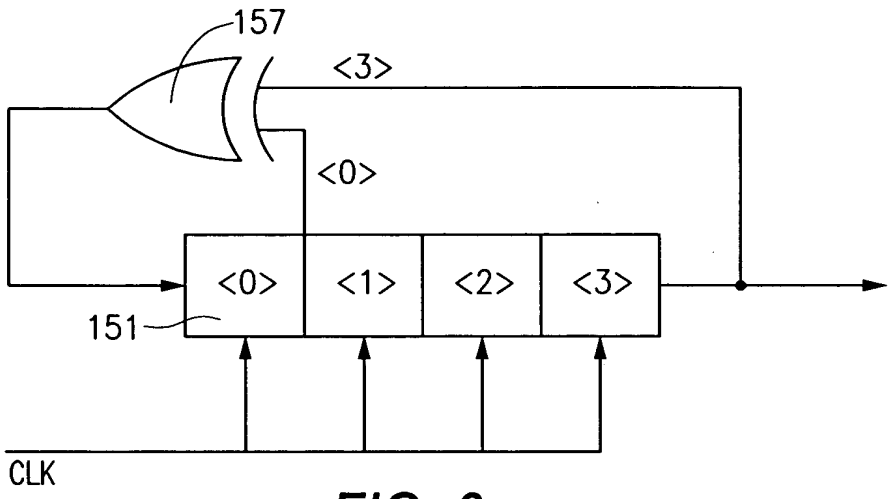

FIG. 6

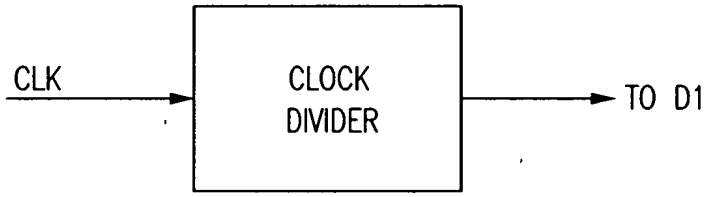

FIG. 7

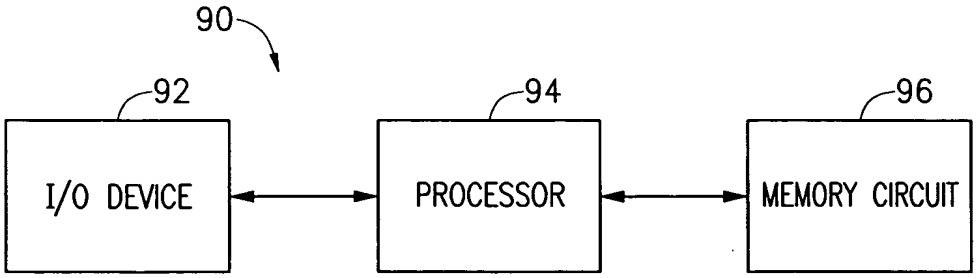

FIG. 8

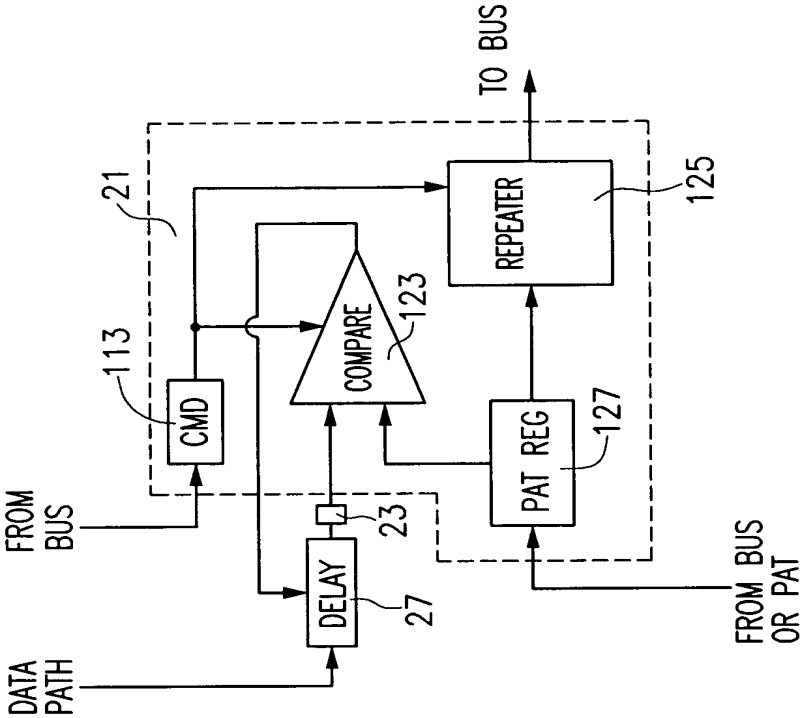
TO BUS
21
REPEATER
125
COMPARE
123
113
CMD
PAT REG
127
FROM BUS
23
DELAY
27
DATA PATH
FROM BUS OR PAT

FIG. 9B

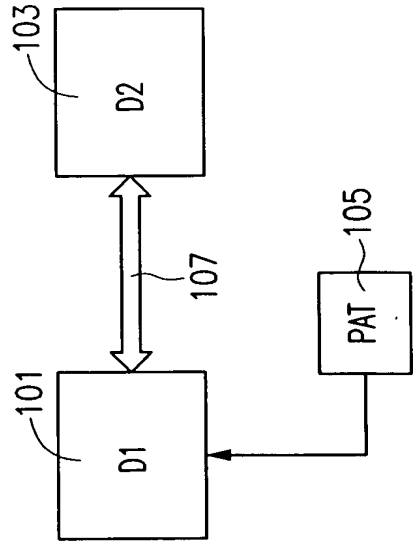
103
D2
107
105
PAT
101
D1

FIG. 9A

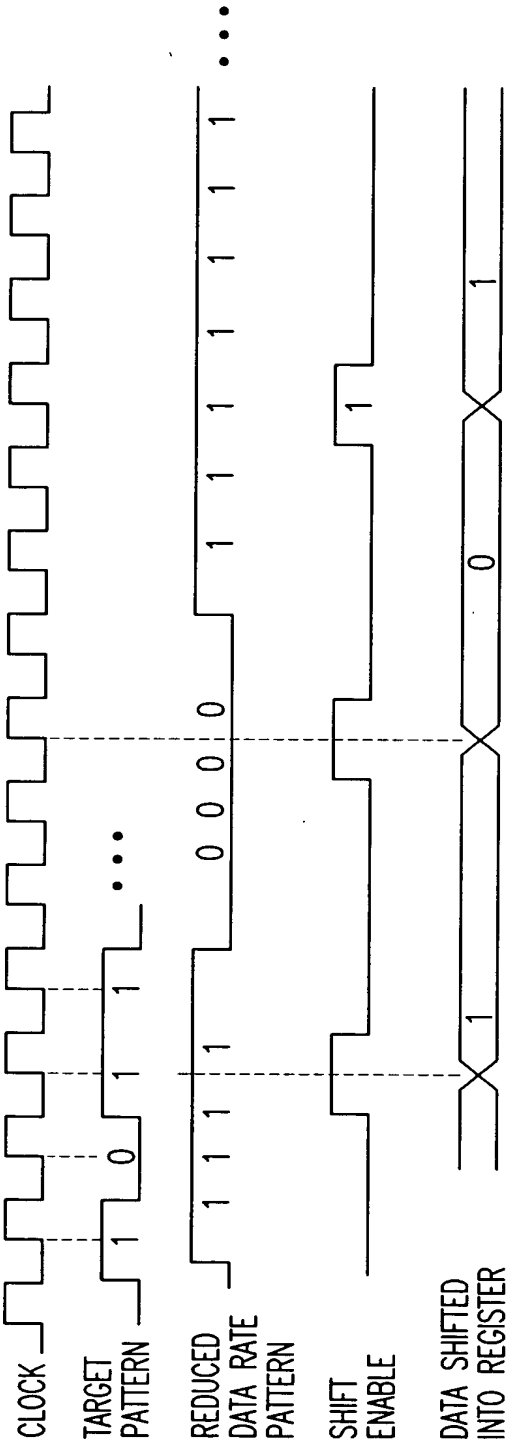

FIG. 10A

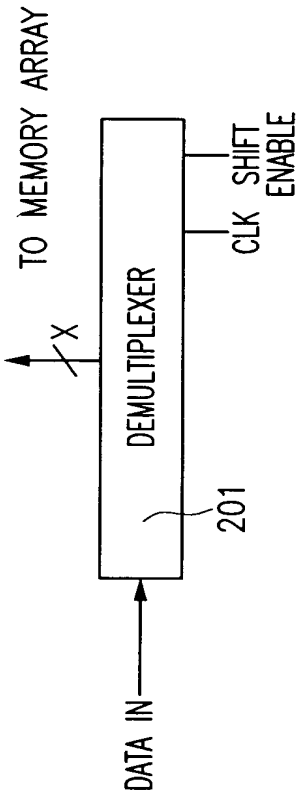

FIG. 10B

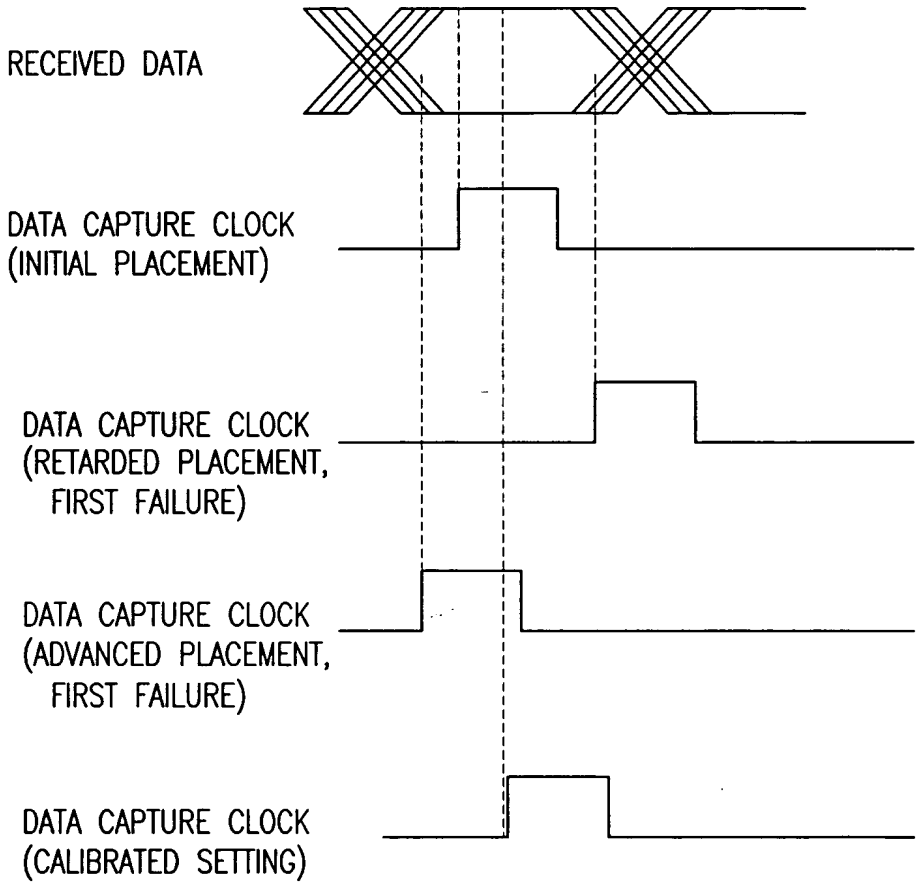
RECEIVED DATA
DATA CAPTURE CLOCK (INITIAL PLACEMENT)
DATA CAPTURE CLOCK (RETARDED PLACEMENT, FIRST FAILURE)
DATA CAPTURE CLOCK (ADVANCED PLACEMENT, FIRST FAILURE)
DATA CAPTURE CLOCK (CALIBRATED SETTING)

FIG. 11

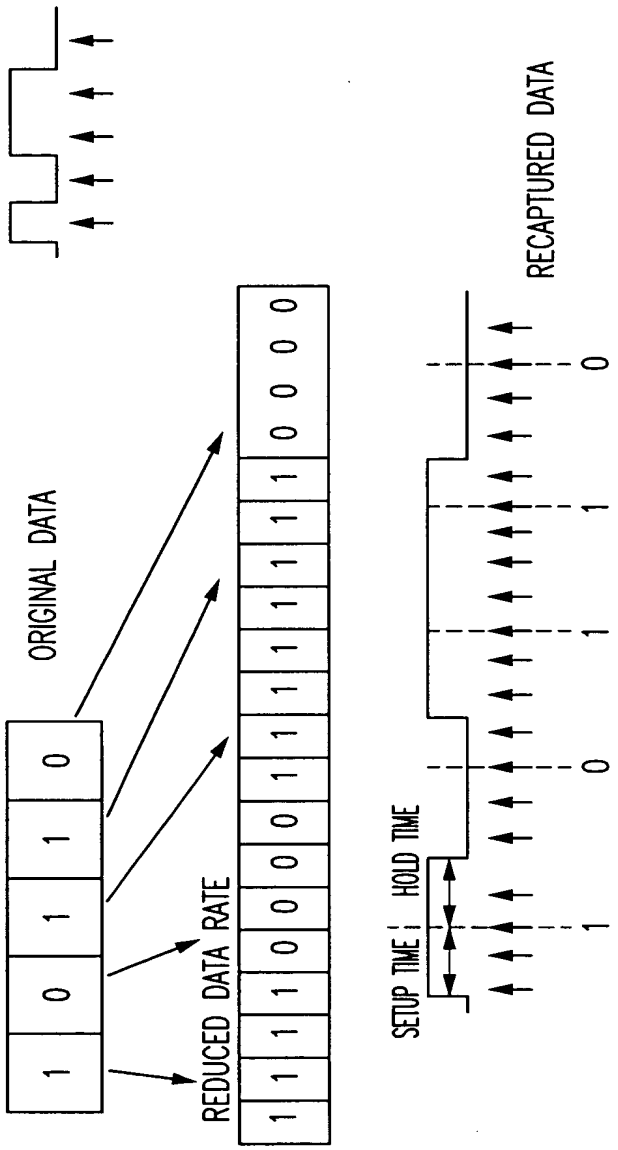
ORIGINAL DATA
1 0 1 1 0
REDUCED DATA RATE
1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 0 0 0 0
SETUP TIME
HOLD TIME
RECAPTURED DATA
1 0 1 1 0

FIG. 12

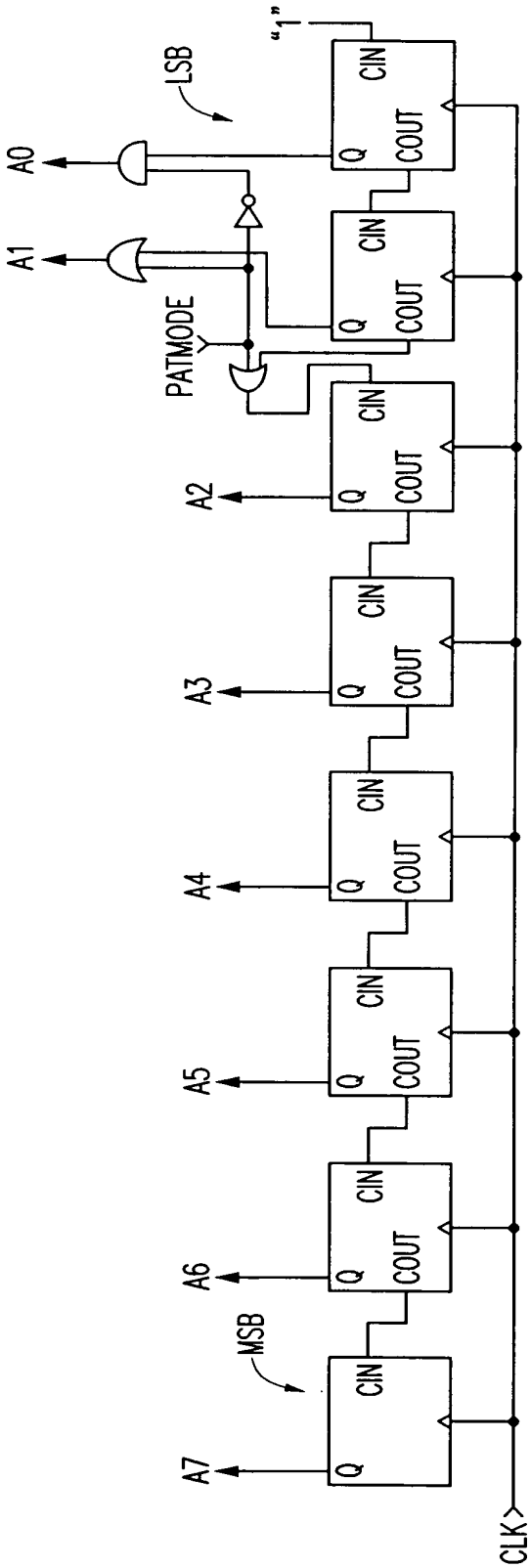

FIG. 13

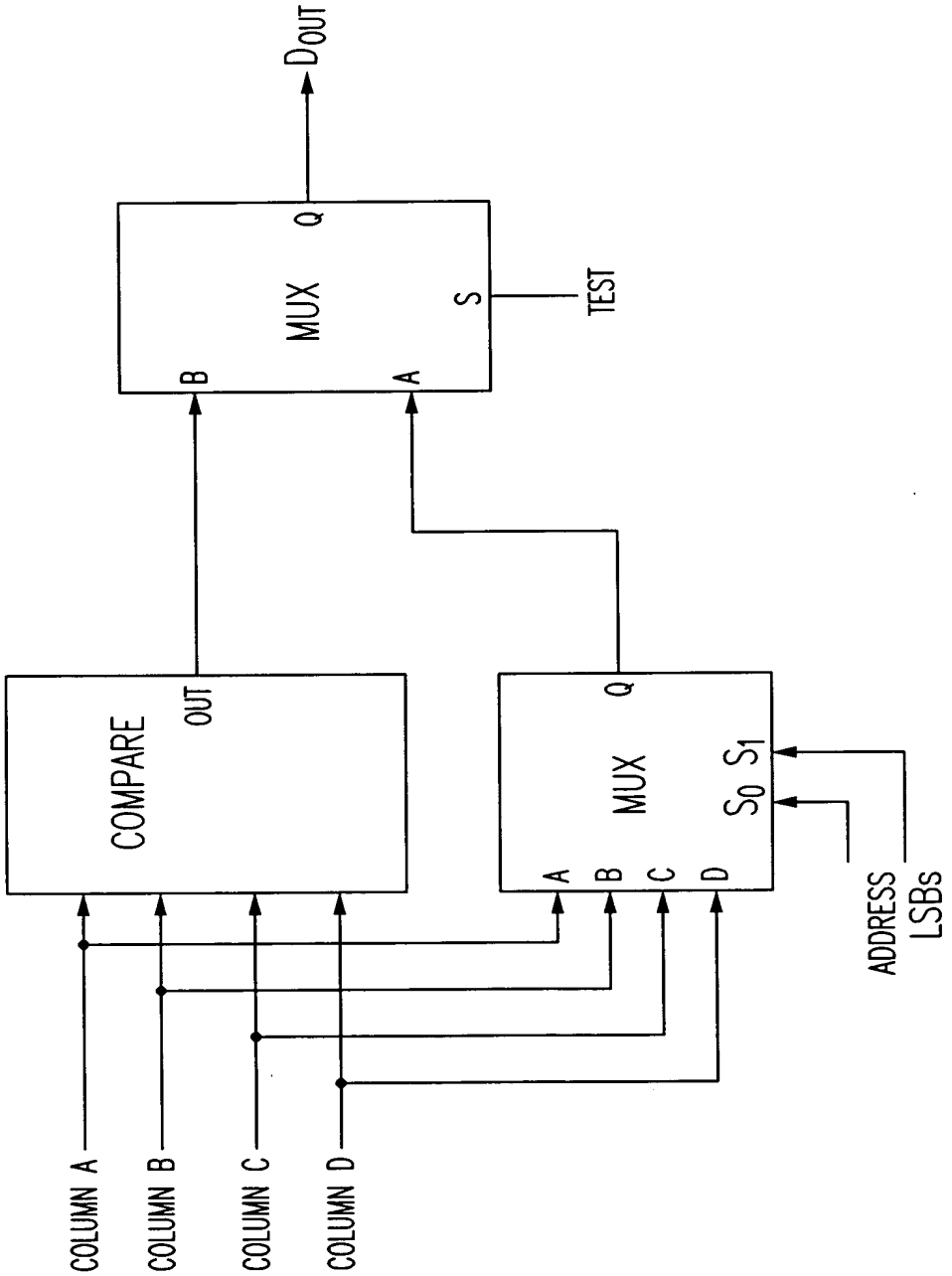
DOUT
Q
MUX
S
TEST
B
A
COMPARE
OUT
Q
MUX
S0 S1
A
B
C
D
ADDRESS LSBs
COLUMN A
COLUMN B
COLUMN C
COLUMN D

FIG. 14A

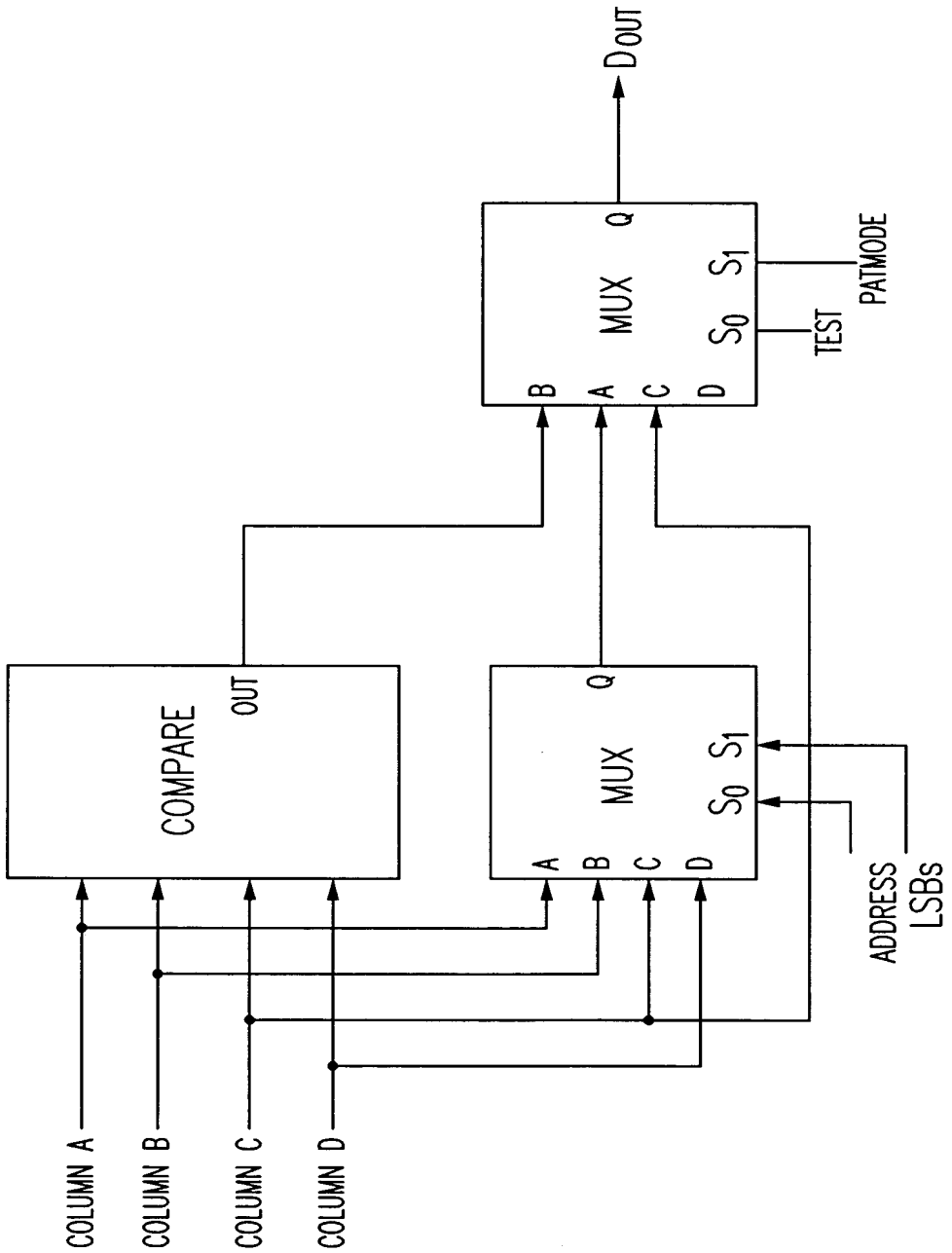
DOUT
MUX
Q
S1
S0
TEST
PATMODE
B
A
C
D
COMPARE
OUT
MUX
Q
S1
S0
A
B
C
D
ADDRESS LSBs
COLUMN A
COLUMN B
COLUMN C
COLUMN D

FIG. 14B

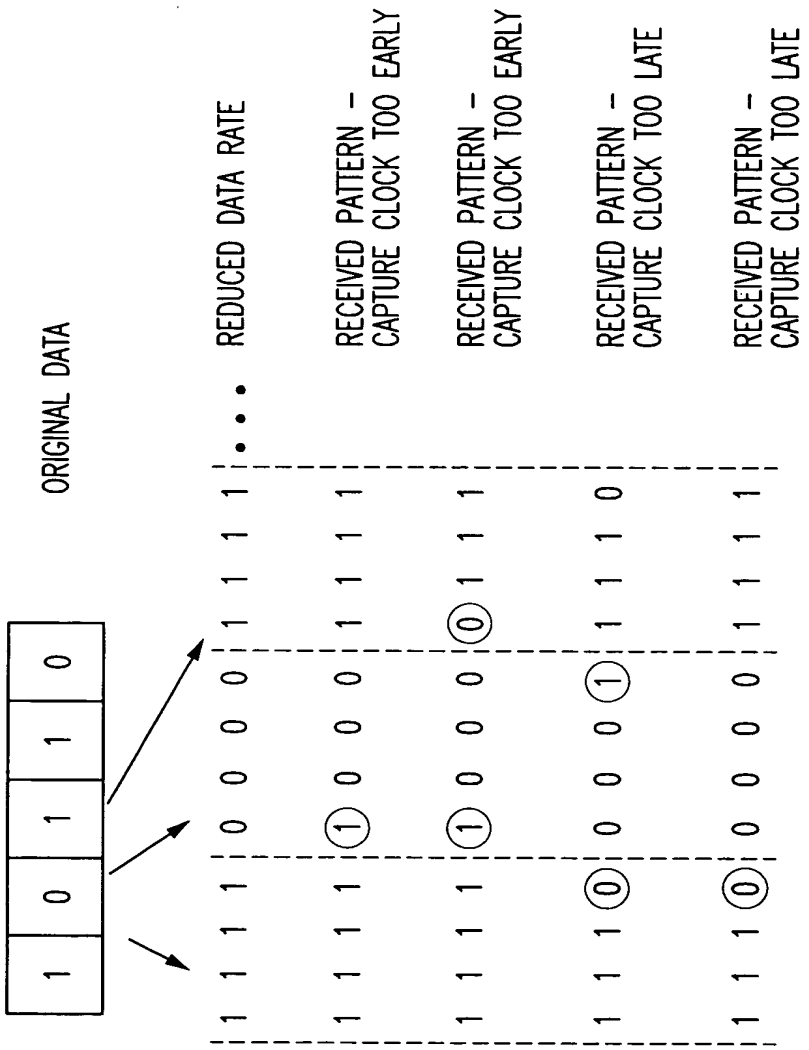
ORIGINAL DATA
REDUCED DATA RATE
RECEIVED PATTERN – CAPTURE CLOCK TOO EARLY
RECEIVED PATTERN – CAPTURE CLOCK TOO EARLY
RECEIVED PATTERN – CAPTURE CLOCK TOO LATE
RECEIVED PATTERN – CAPTURE CLOCK TOO LATE

FIG. 15